

Advancing Wireless Prototyping with Software Defined Radio

Updated Sep 27, 2022

概览

The proliferation of wireless devices for an ever-growing set of applications is driving up the complexity of requirements and designs. Demand for more data is pushing hardware designs toward wider bandwidths, higher frequencies, and more channels, while software is tasked with delivering greater flexibility and shorter time to market.

Whether prototyping new wireless technologies in the lab or evaluating systems in real-world environments, [software defined radios \(SDRs\)](#) offer an ideal solution to ensure performance and design goals are met.

This article introduces the NI [Ettus USRP X410](#) and applications for its use. This Universal Software Radio Peripheral (USRP) is designed to address the latest advanced wireless needs for commercial communications and defense applications from research to deployment.

Contents

- [The Evolution of Wireless Prototyping](#)
- [A New Generation of Software Defined Radio](#)
- [An Open Platform to Enable Your Next Innovation](#)
- [RF Hardware Designed to Scale](#)
- [Summary](#)
- [Next Steps](#)

The Evolution of Wireless Prototyping

In rapidly evolving applications such as drone defense and signal intelligence, faster deployment and the ability to quickly adapt are key. Commercial off-the-shelf (COTS) systems with powerful RF and signal processing capabilities are required, but an open platform is also a must to enable flexible enhancements to stay ahead of threats. For deployment use cases, low size, weight, and power (SWAP) SDRs enable mobile-ready, portable solutions.



Figure 1. SkySafe defeats commercial drone threats fast with open-source USRP.

Commercial wireless communications testbeds and prototypes often need to address multiple frequency bands and standards for cellular and wireless connectivity. Keeping pace with new wireless standards like 5G means developing and testing software IP on capable hardware to prove out technologies that range from new coding schemes to advanced multiple input, multiple output (MIMO) systems often through over-the-air (OTA) wireless prototyping.



联系专家

Figure 2. These low-profile SDRs feature the performance to enable large-scale 5G testbeds.

A New Generation of Software Defined Radio

The NI Ettus USRP X410 is the first of a new generation of high-performance SDRs from Ettus Research and NI. It combines the strength of both NI and Ettus Research into a single radio that supports both popular open-source tool flows, including the USRP Hardware Driver (UHD) and GNU Radio, as well as LabVIEW software. The NI Ettus USRP X410 is built on the Xilinx Zynq UltraScale+ RFSoc and outfitted with high-performance RF transmitter and receiver hardware to deliver NI’s most powerful SDR to date. The RFSoc provides a foundation of embedded processor and programmable FPGA technology integrated with data converters (ADCs/DACs). The quad-core Arm® processor allows for stand-alone operation (embedded mode) or host-based mode with an external host machine to run your application.



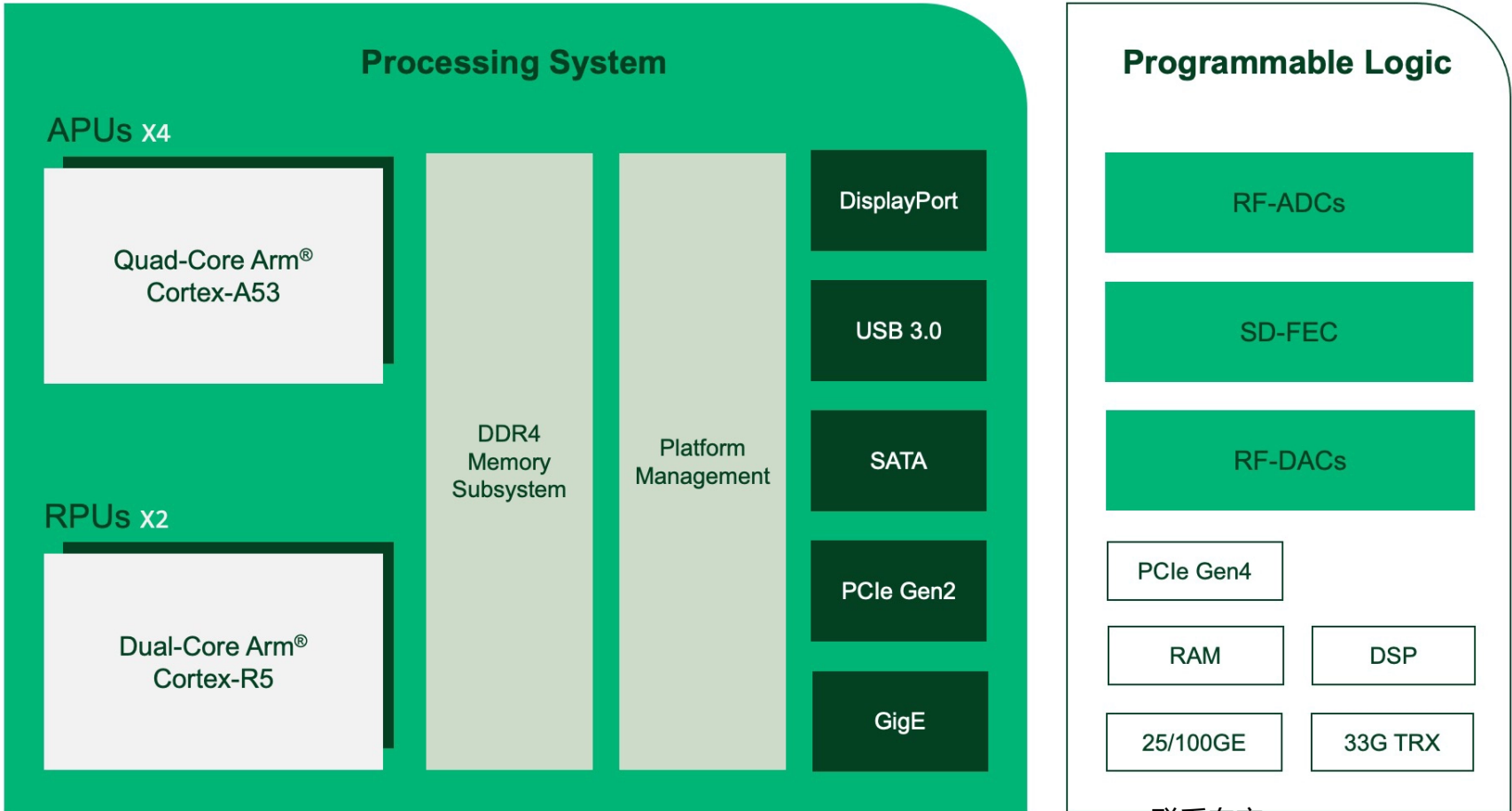
Figure 3. The NI Ettus USRP X410 integrates hardware and software to help you prototype high-performance wireless systems.

An Open Platform to Enable Your Next Innovation

With more than twice the FPGA resources of other USRP products, the programmable logic portion of the Xilinx Zynq UltraScale+ FPGA offers high-throughput digital signal processing (DSP) and hardened IP cores such as an onboard soft-decision forward error correction (SD-FEC) and digital up/down conversion (DUC/DDC) cores. Especially effective for 5G prototyping, the SD-FECs can be used for real-time low-density parity-check (LDPC) encoding/decoding, one of the most compute-intensive operations in 5G. In FPGA-only designs, the SD-FEC logic can span multiple large Virtex-7 FPGAs; thus, incorporating it as a prebuilt core in silicon saves immense space and development effort.

The NI Ettus USRP X410 fully supports the popular RF Network-on-Chip (RFNoC) framework, making FPGA acceleration more accessible with a software application programming interface and FPGA infrastructure. This helps you get up and running quickly so you can focus on the value-added IP. You can seamlessly integrate host-based and FPGA-based processing into your application with the GNU Radio graphical interface, C++, or Python. The library of RFNoC blocks for common functions such as fast Fourier transforms (FFTs) and finite impulse response (FIR) filters is a good place to start. Then you can add your own IP blocks to the modular architecture using your preferred hardware description language (HDL).

Beyond the FPGA fabric portion of the system, the Xilinx UltraScale+ RFSoc is equipped with four onboard application processing units (APUs) and two real-time processing units (RPU) for applications that require an onboard embedded OS for stand-alone operation.



联系专家 >

Figure 4. The simplified block diagram of the Xilinx UltraScale+ RFSoc shows the onboard APUs and RPU for applications that require an onboard embedded OS for stand-alone operation.

RF Hardware Designed to Scale

With a frequency range covering 1 MHz to 7.2 GHz, the NI Ettus USRP X410 addresses not just the traditional RF sub-6 GHz bands but also the recently opened unlicensed band from 5.925 GHz to 7.125 GHz for Wi-Fi 6E. With the 400 MHz instantaneous bandwidth, you can exploit the wider channels and implement channel bonding and carrier aggregation for higher data throughput. The RF front-end architecture uses superheterodyne two-stage conversion below 3 GHz and single-stage conversion above 3 GHz, along with filtering and power-level control, to provide high-fidelity signal transmit and receive.

The NI Ettus USRP X410 incorporates four transmit and four receive channels into a compact ½ rack 1U form factor, making it versatile and easily transportable for field testing and operations. Each channel is independent, meaning each can be tuned to different frequencies for frequency division duplex (FDD) applications or for the simultaneous emulation of multiple signals. The channels can also be synchronized through an internal oven-controlled crystal oscillator (OCXO) that you can calibrate to within 50 ppb, an internal GPS disciplined oscillator (GPSDO) for time stamping, and 10 MHz reference and pulse-per-second (PPS) generation. For even higher channel counts, you can synchronize multiple devices by importing an external reference clock and using PPS generation for applications that require precise time alignment such as massive MIMO.

With wider bandwidths and more channels, moving a large amount of data on and off the radio can be a challenge. To address this, the NI Ettus USRP X410 features two configurable quad small form-factor pluggable (QSFP) ports that you can use to take advantage of dual 10 GbE or dual 100 GbE onboard. Additionally, the radio includes a PCI Express x8 Gen 3 port for up to 8 GB/s transfer rates.

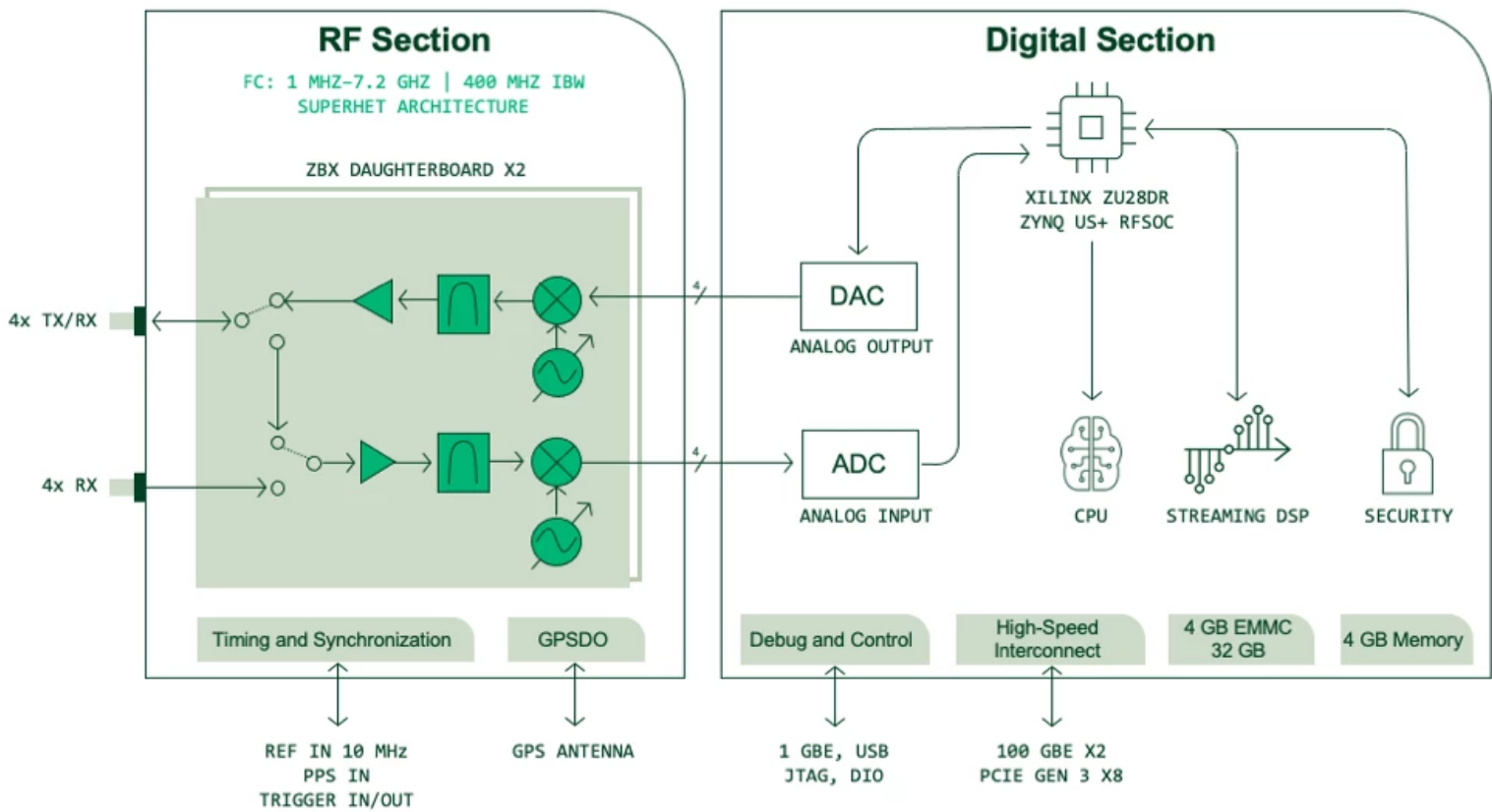


Figure 5. The block diagram of the NI Ettus USRP X410 shows its RF and digital functions.

Summary

The powerful performance of the NI Ettus USRP X410 offers an ideal platform to build your latest innovation. Paired with your choice of software toolchain, this software defined radio has the capability and flexibility to meet your needs. Whether you are performing research for 5G and beyond or deploying systems to mitigate advancing threats, the NI Ettus USRP X410 can accelerate your wireless device prototyping.

Next Steps

- [See the NI Ettus USRP X410 in Action](#)
- [Choose the Right USRP for Your Application](#)
- [Learn what's next in software defined radio research](#)